NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

[An Institute of National Importance under Ministry of Education, Govt. of India]

Sector 1, Rourkela, Sundergarh Dist., Odisha 769 008

SPONSORED RESEARCH INDUSTRIAL CONSULTANCY CONTINUING EDUCATION

NITR / SR / 2024 / Advt.- 23EC012 / L / 015   dt. 03/05/2024 Ref: FTS 8032AA   **SR-R03**

Advertisement for Recruitment of Project Position

Candidates who fulfill the below mentioned criteria may submit the application form before the last date. Engagement will be purely on temporary / contractual basis and co-terminus with the completion of the project. Candidates are advised to go through the advertisement details carefully before applying.

1.	Title of the Project:	Design and development of SoC for Industry 4.0 with Functional safety and security	
2.	Project Code with Duration *(Closing Date)*:	**SR/23/EC/012**	**10/02/2027**
3.	Funding Agency Details:	MEITY	-
4.	Department / Centre:	Dept. of **Electronics and Communication Engg.**	

5.	Name of the PI with details:	Prof. **Kamalakanta Mahapatra**		Prof. **Ayas Kanta Swain**	
		kkm @nitrkl.ac.in	- @ gmail.com	swaina @nitrkl.ac.in	- @ gmail.com
		0661-246 2454 -	-	0661-246 2458 9437341298	-

6. Details of the Post(s):   **7. Educational Qualification & Working Knowledge**

Senior Project Associate

[Name of the Post(s)]

01 (One)	**03** Year(s), **00** Month(s)
[No. of Post(s)]	*(Tenure of Post)*

Year 1 & 2

INR **54,000.00** /- per month
(+) HRA @ **NA** % (if applicable)

Year 3

INR **65,340.00** /- per month
(+) HRA @ **NA** % (if applicable)

Essential Qualification (s):

Ph.D in VLSI design or related discipline / M.Tech having 3 years of experience in VLSI design, and research paper publication with 65% marks or 7.0 CGPA along with Institute norms.

Desirable Qualification:

Experience of chip tape-out and IC testing. Applicants with GATE score will be preferable.

Experience / Software / Skillset:

Experience in the area of Hardware security, functional safety in industrial IoT, product design and field testing. Knowledge of Verilog, RTL coding and driver development using C language.

Job Description:

Carry out research in the area of IC design, test and product development for industry 4.0.
Coordinate with cluster institutes for project activities and attend trainings.
Maintain EDA tools and workstations in laboratories and support students in the related area.
Create essential documentation for project and manuals for EDA tools.
Assisting PIs for various activities towards completion of the Chips to Startup project.

Applicants (with M.Tech) are expected to pursue a PhD in ECE Dept satisfying the Institute Eligibility Criteria.

Online   Interview details: **24/05/2024**   **9.30 AM**   **Department of Electronics and Communication Engg.**

Application link for eligible candidate(s): NIT Rourkela Homepage ➡ FACULTY & STAFF ➡ SRICCE ➡ Career ➡ Notices

The candidate(s) are required to send the complete filled and signed application (soft copy) with documents regarding educational qualification indicating percentage of marks / division (mark-sheets and / or certificates), research papers (if any), work experience certificate (if any) etc., This may be built as a single PDF file and sent by email with "Advertisement No." on the subject link to the above mentioned e-mail IDs. NO hard copies of application(s) are required to be sent to the Institute.

Last date for submitting the Application: 21/05/2024

The period of experience in a discipline / area of work, wherever prescribed, shall be counted after the date of acquiring the minimum prescribed educational qualifications for that position. Mere possession of minimum qualification does not guarantee invitation to the interview. Candidates will be short listed based on merit and need of the project. Selection / Joining will be cancelled in case of any suppression of information / document submitted.

NIT Rourkela reserves the right to fix higher criteria for short-listing of eligible candidates from those satisfying advertised qualification and requirement of the project post. Only short-listed candidates will be informed for Online interview. In case, any clarification is required on eligibility regarding the above post, the candidate may contact in the above mentioned details.

Age Guideline:

The upper age limit for applying for the award of project position shall be 28 years, which is relaxed up to 5 years in the case of candidates belonging to Schedule Castes / Schedule Tribes / PWD and Female applicants whereas 3 years in the case of OBCs (Non-creamy layer candidates). Upper age limit shall be reckoned as on the last date of receipt of applications.

Any other terms & conditions governed as per guidelines issued by the funding agency for the engagement of above position as amended from time to time shall be in force towards this temporary recruitment.

Sd/-
Asst. / Dy. / Jt. Registrar (SR)

Copy to:
- PI   : **Prof.** Kamalakanta Mahapatra , Dept. of **EC**
- Co-PI : **Prof.** Ayas Kanta Swain , Dept. of **EC**
- Chairman, DRC, Dept. of **EC**
- Head of the Department / Centres / Units ➡ It is requested that the contents of the above advertisement be brought to the notice of the staff(s) / student(s) working in your Deptt. / Centre / Unit.
- Dealing Seat (SR – Project Recruitment) ➡ *To publish advertisement at NITR website.*
- Advertisement File